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Question Paper Code : 90174

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER / DECEMBER 2019

Third Semester

Electronics and Communication Engineering

EC8351 – ELECTRONIC CIRCUITS – I

(Common to Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Mention any two biasing circuits of BJT.
2. Find the operating region of n-channel MOSFET with $V_{GS} = 1V$, $V_t = 0.8 V$ and $V_{DS} = 1.2 V$.
3. What is meant by base width modulation ?
4. What is the overall gain of 3-stage cascaded amplifier, having individual gain of amplifier is 20 V/V ?
5. Derive the output resistance of CS amplifier.
6. What are the features of BiCMOS circuits ?
7. List the effect of capacitors that effect frequency response of BJT.
8. Draw the high frequency equivalent circuit of MOSFET.
9. Derive ripple factor of full wave bridge rectifier.
10. Define load regulation of regulators.



PART - B

(5×13=65 Marks)

11. a) For the circuit in Fig. 1 draw DC load line and find the Q-point. $h_{fe} = 150$, $V_{cc} = 15\text{ V}$, $R_C = 2100\ \Omega$, $R_1 = 566\ \text{K}\Omega$, $R_2 = 120\ \text{K}\Omega$, $V_{BE-on} = 0.7\text{ V}$, $I_B = 10\ \mu\text{A}$.

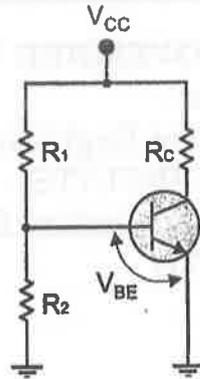


Fig. 1

(OR)

- b) For the circuit in Fig. 2, find the drain current and drain to source voltage. MOSFET is operating in saturation region.

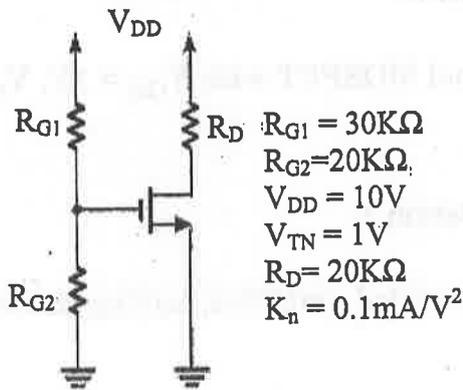


Fig. 2

12. a) Derive gain of common emitter amplifier circuits with R_E bypassed by C_E , draw the small signal equivalent circuit.

(OR)

- b) With equivalent circuit, derive the input impedance of Bootstrapped Darlington amplifier.

13. a) Derive gain, input and output impedance of common drain amplifier with neat circuit diagram and equivalent circuit.

(OR)

- b) Derive CMRR and explain the operation of differential pair using FET with circuit diagram.

14. a) Derive f_{α} and f_{β} of a frequency response of BJT.

(OR)

b) Derive expressions for high frequency analysis of CE and MOSFET CS amplifiers.

15. a) Draw the circuit of shunt voltage regulator and explain its operation.

(OR)

b) Explain the functional blocks of Switched Mode Power Supply (SMPS).

PART - C

(1×15=15 Marks)

16. a) For the circuit shown in Fig. 3, identify the amplifier configuration, find the input and output resistance $V_{BE} = 0.7V$, $V_A = 80 V$, $\beta = 100$.

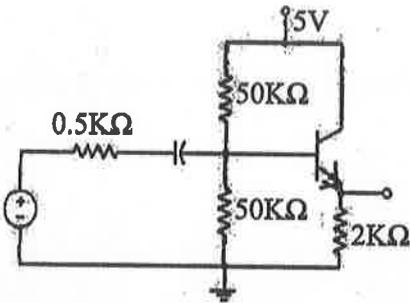


Fig. 3

(OR)

b) Determine the Unity gain bandwidth, Miller capacitance and cut-off frequency of Common source MOSFET circuit. $V_T = 1V$, $V_{GS} = 3V$, $K_n = 0.25mA/V^2$, $R_L = 10 K\Omega$, $C_{gd} = 0.04pF$, $c_{gs} = 0.2 pF$.

